

XC822/824

8-Bit Single-Chip Microcontroller

Data Sheet

V1.2 2011-10

Microcontrollers

Edition 2011-10

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Data Sheet

V1.2 2011-10

Microcontrollers

XC822/824 Data Sheet**Revision History: V1.2 2011-10**

Previous Versions: V1.1

| Page | Subjects (major changes since last revision) |
|----------------|---|
| Page 3 | A new variant (SAK-XC822MT-0FRA) was added in Table 2. |
| Page 19 | Added a new chip identification number for variant (SAK-XC822MT-0FRA) in Table 5. |

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1 Summary of Features

The XC822/824 has the following features:

- High-performance XC800 Core
 - compatible with standard 8051 processor
 - two clocks per machine cycle architecture (for memory access without wait state)
 - two data pointers
- On-chip memory
 - 8 Kbytes of Boot ROM, Library ROM and User routines
 - 256 bytes of RAM
 - 256 bytes of XRAM
 - 2/4 Kbytes of Flash (includes memory protection strategy)
- I/O port supply at 2.5 V - 5.5 V and core logic supply at 2.5 V (generated by embedded voltage regulator)

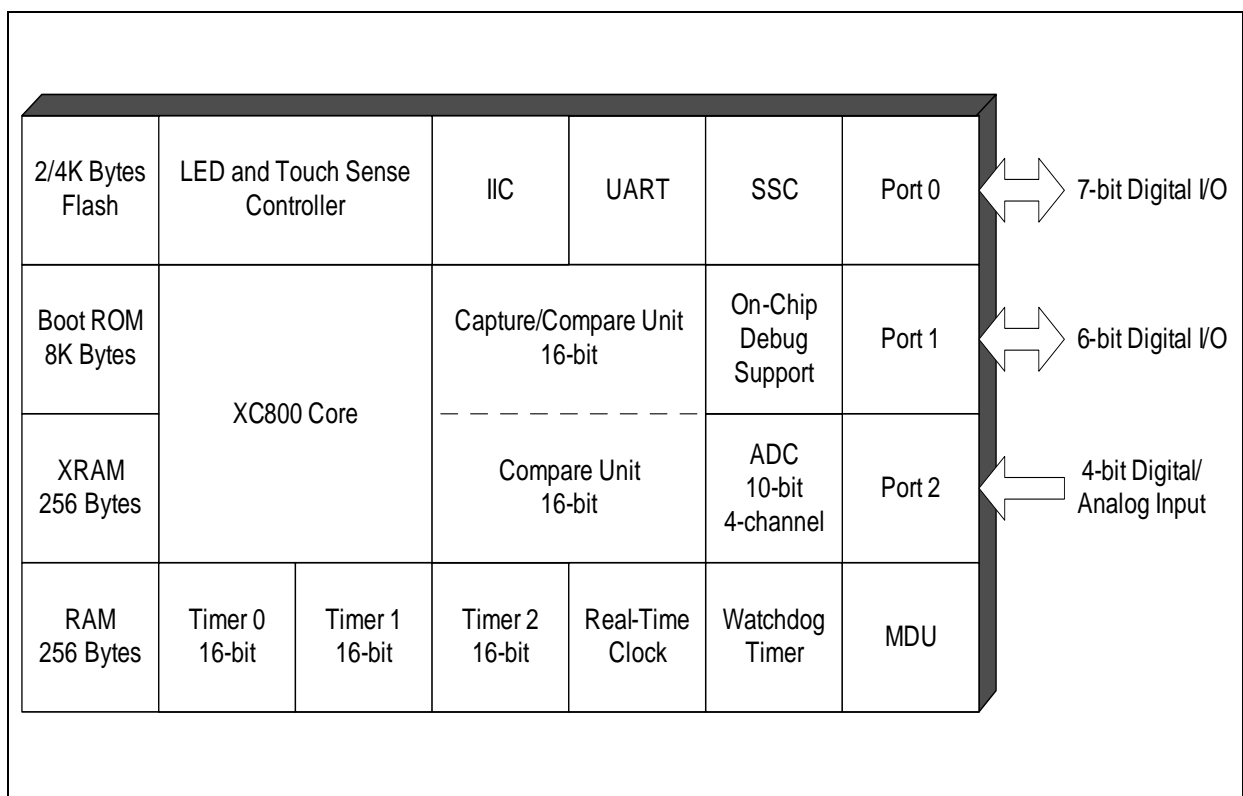


Figure 1 XC822/824 Functional Units

- Power-on reset generation
- Brownout detection for IO supply and core logic supply
- 48 MHz on-chip OSC for clock generation
 - Loss-of-Clock detection

(more features on next page)

Summary of Features

Features: (continued)

- Power saving modes
 - idle mode
 - power-down mode with wake-up capability via real-time clock interrupt
 - clock gating control to each peripheral
- Programmable 16-bit Watchdog Timer (WDT) running on independent oscillator with programmable window feature for refresh operation and warning prior to overflow
- Three ports
 - Up to 17 pins as digital I/O
 - 4 pin as digital/analog input
- 4-channel, 10-bit ADC
 - support up to 3 differential input channel
 - results filtering by data reduction or digital low-pass filter, for up to 13-bit results
- Up to 4 channels, Out of range comparator
- Three 16-bit timers
 - Timer 0 and Timer 1 (T0 and T1)
 - Timer 2 (T2)
- Periodic wake-up timer
- Multiplication/Division Unit for arithmetic operations (MDU)
- Capture and Compare unit for PWM signal generation (CCU6)
- A full-duplex or half-duplex serial interface (UART)
- Synchronous serial channel (SSC)
- Inter-IC (IIC) serial interface
- LED and Touch-sense Controller (LEDTSCU)
- On-chip debug support via single pin DAP interface (SPD)
- Packages:
 - PG-DSO-20
 - PG-TSSOP-16
- Temperature range T_A :
 - SAF (-40 to 85 °C)
 - SAX (-40 to 105 °C)
 - SAK (-40 to 125 °C)

Summary of Features
XC822/824 Variant Devices

The XC822/824 product family features devices with different configurations, program memory sizes, packages options and temperature profiles, to offer cost-effective solutions for different application requirements.

The list of XC822/824 device configurations are summarized in [Table 1](#). The type of packages available are TSSOP-16 for XC822 and DSO-20 for XC824.

Table 1 Device Configuration

| Device Name | MDU Module | LEDTSCU Module |
|-------------|------------|----------------|
| XC822/824 | No | No |
| XC822/824M | Yes | No |
| XC822/824T | No | Yes |
| XC822/824MT | Yes | Yes |

[Table 2](#) shows the device sales type available, based on above device.

Table 2 Device Profile

| Sales Type | Device Type | Program Memory (Kbytes) | Temperature Profile (°C) | Package Type | Quality Profile |
|------------------|-------------|-------------------------|--------------------------|--------------|-----------------|
| SAF-XC822T-0FRI | Flash | 2 | -40 to 85 | PG-TSSOP-16 | Industrial |
| SAF-XC822-1FRI | Flash | 4 | -40 to 85 | PG-TSSOP-16 | Industrial |
| SAF-XC822T-1FRI | Flash | 4 | -40 to 85 | PG-TSSOP-16 | Industrial |
| SAF-XC822M-1FRI | Flash | 4 | -40 to 85 | PG-TSSOP-16 | Industrial |
| SAF-XC822MT-1FRI | Flash | 4 | -40 to 85 | PG-TSSOP-16 | Industrial |
| SAF-XC824M-1FGI | Flash | 4 | -40 to 85 | PG-DSO-20 | Industrial |
| SAF-XC824MT-1FGI | Flash | 4 | -40 to 85 | PG-DSO-20 | Industrial |
| SAX-XC824M-1FGI | Flash | 4 | -40 to 105 | PG-DSO-20 | Industrial |
| SAK-XC824M-1FGI | Flash | 4 | -40 to 125 | PG-DSO-20 | Industrial |
| SAF-XC822-1FRA | Flash | 4 | -40 to 85 | PG-TSSOP-16 | Automotive |
| SAF-XC822MT-1FRA | Flash | 4 | -40 to 85 | PG-TSSOP-16 | Automotive |
| SAK-XC822MT-0FRA | Flash | 2 | -40 to 125 | PG-TSSOP-16 | Automotive |
| SAK-XC822-1FRA | Flash | 4 | -40 to 125 | PG-TSSOP-16 | Automotive |
| SAK-XC822MT-1FRA | Flash | 4 | -40 to 125 | PG-TSSOP-16 | Automotive |

Summary of Features

As this document refers to all the derivatives, some description may not apply to a specific product. For simplicity, all versions are referred to by the term XC822/824 throughout this document.

Ordering Information

The ordering code for Infineon Technologies microcontrollers provides an exact reference to the required product. This ordering code identifies:

- The derivative itself, i.e. its function set, the temperature range, and the supply voltage
- The package and the type of delivery

For the available ordering codes for the XC822/824, please refer to your responsible sales representative or your local distributor.

2 General Device Information

Chapter 2 contains the block diagram, pin configurations, definitions and functions of the XC822/824.

2.1 Block Diagram

The block diagram of the XC822/824 is shown in **Figure 2**.

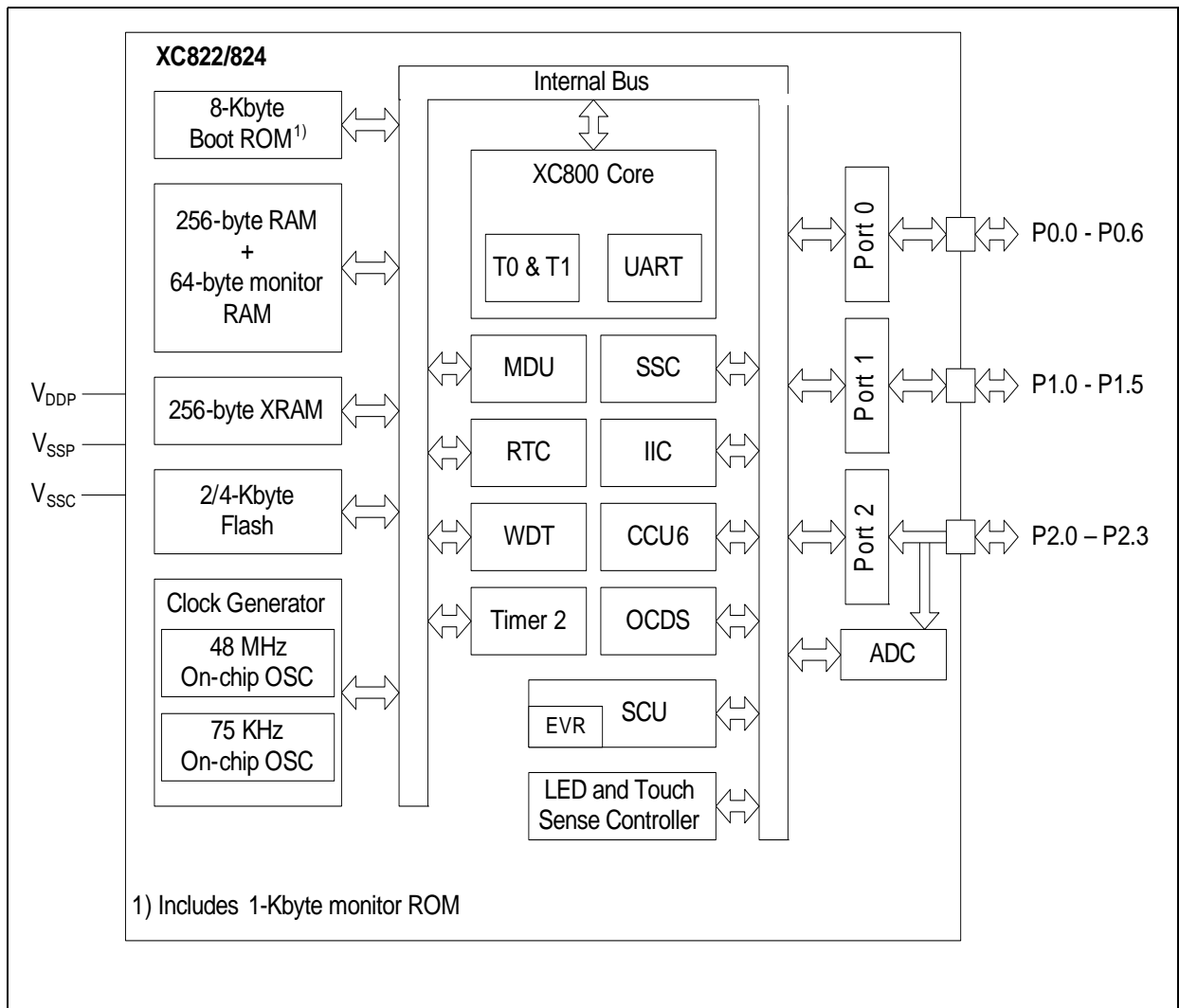


Figure 2 XC822/824 Block Diagram

2.2 Logic Symbol

The logic symbol of the XC822/824 is shown in [Figure 3](#).

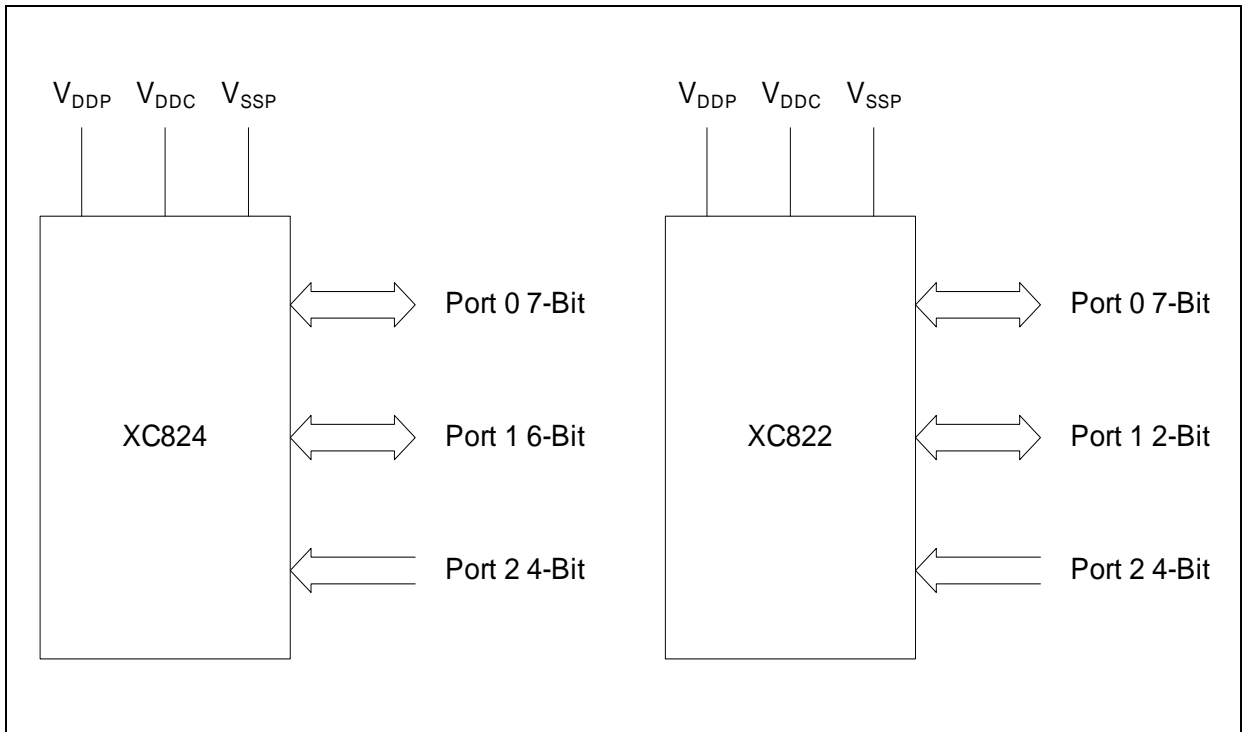


Figure 3 XC822/824 Logic Symbol

2.3 Pin Configuration

The pin configuration of the XC822 in [Figure 4](#).

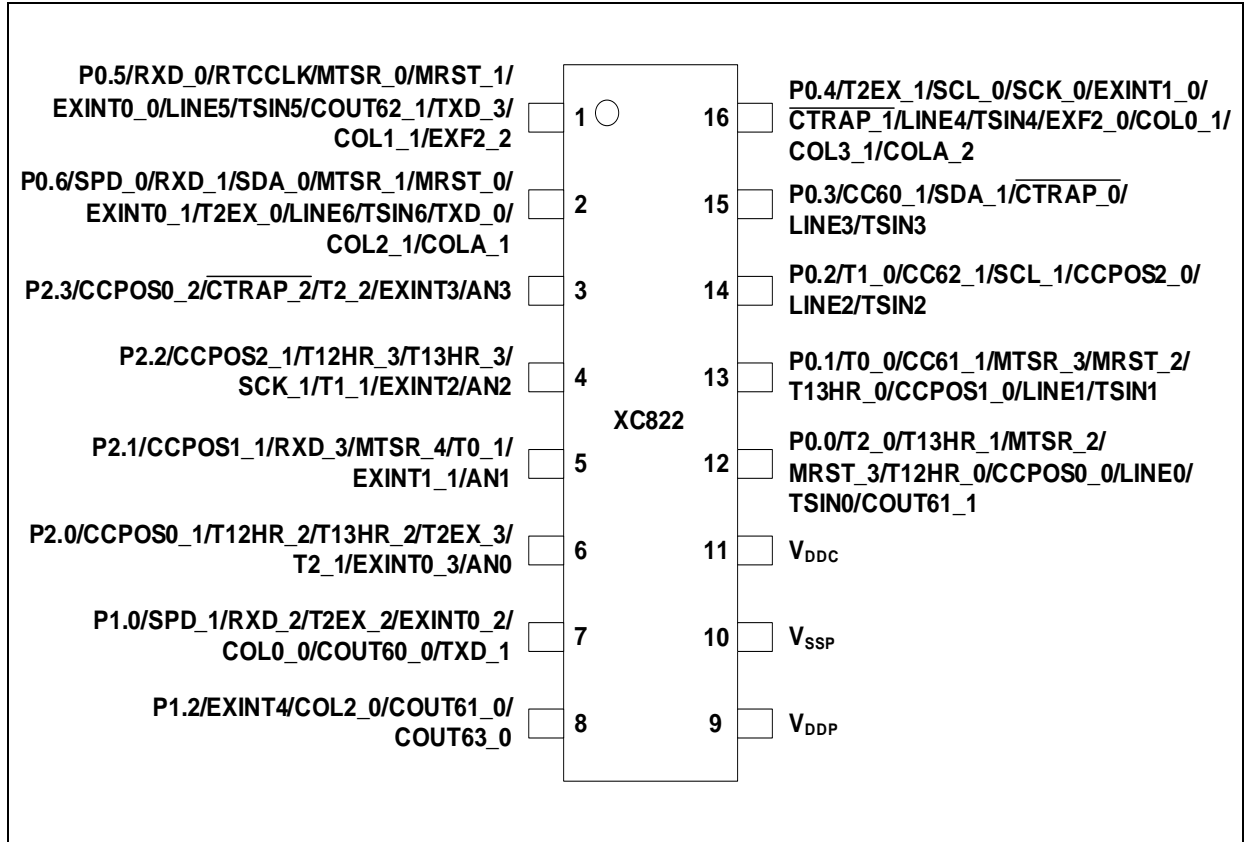


Figure 4 XC822 Pin Configuration, PG-TSSOP-16 Package (top view)

General Device Information

The pin configuration of the XC824 in [Figure 5](#).

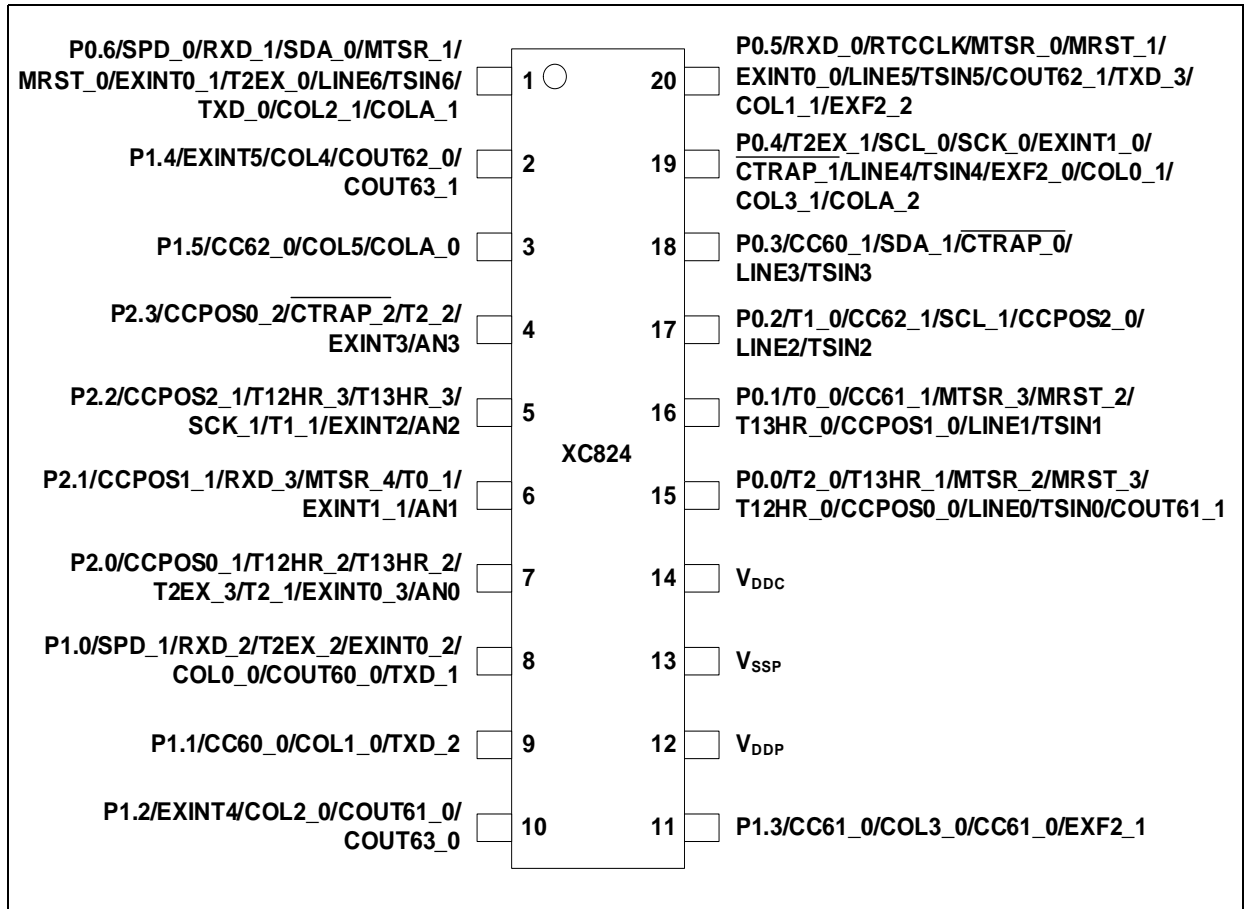


Figure 5 XC824 Pin Configuration, PG-DSO-20 Package (top view)

2.4 Pin Definitions and Functions

The functions and default states of the XC822/824 external pins are provided in [Table 3](#).

Table 3 Pin Definitions and Functions for XC822/824

| Symbol | Pin Number DSO20/ TSSOP16 | Type | Reset State | Function |
|--------|---------------------------------|------|-------------|--|
| P0 | | I/O | | <p>Port 0 Port 0 is a bidirectional general purpose I/O port. It can be used as alternate functions for LEDTSCU, Timer 0, 1 and 2, SSC, CCU6, IIC, SPD and UART.</p> |
| P0.0 | 15/12 | | Hi-Z | <p>T2_0 Timer 2 Input</p> <p>T13HR_1 CCU6 Timer 13 Hardware Run Input</p> <p>MTSR_2 SSC Master Transmit Output/ Slave Receive Input</p> <p>MRST_3 SSC Master Receive Input</p> <p>T12HR_0 CCU6 Timer 12 Hardware Run Input</p> <p>CCPOS0_0 CCU6 Hall Input 0</p> <p>TSIN0 Touch-sense Input 0</p> <p>LINE0 LED Line 0</p> <p>COUT61_1 Output of Capture/Compare Channel 1</p> |

General Device Information
Table 3 Pin Definitions and Functions for XC822/824

| Symbol | Pin Number DSO20/ TSSOP16 | Type | Reset State | Function |
|--------|---------------------------------|------|-------------|---|
| P0.1 | 16/13 | | Hi-Z | T0_0 Timer 0 Input CC61_1 Input/Output of Capture/Compare channel 1 MTSR_3 SSC Slave Receive Input MRST_2 SSC Master Receive Input/ Slave Transmit Output T13HR_0 CCU6 Timer 13 Hardware Run Input CCPOS1_0 CCU6 Hall Input 1 TSIN1 Touch-sense Input 1 LINE1 LED Line 1 |
| P0.2 | 17/14 | | Hi-Z | T1_0 Timer 1 Input CC62_1 Input/Output of Capture/Compare channel 2 SCL_1 IIC Clock Line CCPOS2_0 CCU6 Hall Input 2 TSIN2 Touch-sense Input 2 LINE2 LED Line 2 |
| P0.3 | 18/15 | | Hi-Z | CC60_1 Input/Output of Capture/Compare channel 0 SDA_1 IIC Data Line CTRAP_0 CCU6 Trap Input TSIN3 Touch-sense Input 3 LINE3 LED Line 3 |

General Device Information
Table 3 Pin Definitions and Functions for XC822/824

| Symbol | Pin Number DSO20/ TSSOP16 | Type | Reset State | Function | |
|--------|---------------------------------|------|-------------|-----------|--|
| P0.4 | 19/16 | | PD | T2EX_1 | Timer 2 External Trigger Input |
| | | | | SCK_0 | SSC Clock Input/Output |
| | | | | SCL_0 | IIC Clock Line |
| | | | | CTRAP_1 | CCU6 Trap Input |
| | | | | EXINT1_0 | External Interrupt Input 1 |
| | | | | TSIN4 | Touch-sense Input 4 |
| | | | | LINE4 | LED Line 4 |
| | | | | EXF2_0 | Timer 2 Overflow Flag |
| | | | | COL0_1 | LED Column 0 |
| | | | | COL3_1 | LED Column 3 |
| | | | | COLA_2 | LED Column A |
| P0.5 | 20/1 | | Hi-Z | RXD_0 | UART Receive Input |
| | | | | RTCCLK | RTC External Clock Input |
| | | | | MTSR_0 | SSC Master Transmit Output/ Slave Receive Input |
| | | | | MRST_1 | SSC Master Receive Input |
| | | | | EXINT0_0 | External Interrupt Input 0 |
| | | | | TSIN5 | Touch-sense Input 5 |
| | | | | LINE5 | LED Line 5 |
| | | | | COOUT62_1 | Output of Capture/Compare Channel 2 |
| | | | | TXD_3 | UART Transmit Output/ 2-wire UART BSL Transmit Output |
| | | | | COL1_1 | LED Column 1 |
| EXF2_2 | Timer 2 Overflow Flag | | | | |

General Device Information
Table 3 Pin Definitions and Functions for XC822/824

| Symbol | Pin Number DSO20/ TSSOP16 | Type | Reset State | Function |
|-----------|---------------------------------|------|-------------|--|
| P0.6 | 1/2 | | PU | SPD_0 SPD Input/Output RXD_1 UART Receive Input/ UART BSL Receive Input SDA_0 IIC Data Line MTSR_1 SSC Slave Receive Input MRST_0 SSC Master Receive Input/ Slave Transmit Output EXINT0_1 External Interrupt Input 0 T2EX_0 Timer 2 External Trigger Input TSIN6 Touch-sense Input 6 LINE6 LED Line 6 TXD_0 UART Transmit Output/ 1-wire UART BSL Transmit Output COL2_1 LED Column 2 COLA_1 LED Column A |
| P1 | | I/O | | Port 1 Port 1 is a bidirectional general purpose I/O port. It can be used as alternate functions for CCU6, LEDTSCU, SPD, UART and Timer 2. |
| P1.0 | 8/7 | | Hi-Z | SPD_1 SPD Input/Output RXD_2 UART Receive Input T2EX_2 Timer 2 External Trigger Input EXINT0_2 External Interrupt Input 0 COL0_0 LED Column 0 COUT60_0 Output of Capture/Compare Channel 0 TXD_1 UART Transmit Output |

General Device Information
Table 3 Pin Definitions and Functions for XC822/824

| Symbol | Pin Number DSO20/ TSSOP16 | Type | Reset State | Function |
|-----------|---------------------------------|------|-------------|--|
| P1.1 | 9/- | | Hi-Z | CC60_0 Input/Output of Capture/Compare channel 0 COL1_0 LED Column 1 TXD_2 UART Transmit Output |
| P1.2 | 10/8 | | Hi-Z | EXINT4 External Interrupt Input 4 COL2_0 LED Column 2 COUT61_0 Output of Capture/Compare channel 1 COUT63_0 Output of Capture/Compare channel 3 |
| P1.3 | 11/- | | Hi-Z | CC61_0 Input/Output of Capture/Compare channel 1 COL3_0 LED Column 3 EXF2_1 Timer 2 Overflow Flag |
| P1.4 | 2/- | | Hi-Z | EXINT5 External Interrupt Input 5 COL4 LED Column 4 COUT62_0 Output of Capture/Compare channel 2 COUT63_1 Output of Capture/Compare channel 3 |
| P1.5 | 3/- | | Hi-Z | CC62_0 Input/Output of Capture/Compare channel 2 COL5 LED Column 5 COLA_0 LED Column A |
| P2 | | I | | Port 2 Port 2 is a general purpose input-only port. It can be used as inputs for A/D Converter and out of range comparator, CCU6, Timer 2, SSC and UART. |

General Device Information
Table 3 Pin Definitions and Functions for XC822/824

| Symbol | Pin Number DSO20/ TSSOP16 | Type | Reset State | Function |
|--------|---------------------------------|------|-------------|---|
| P2.0 | 7/6 | | Hi-Z | CCPOS0_1 CCU6 Hall Input 0 T12HR_2 CCU6 Timer 12 Hardware Run Input T13HR_2 CCU6 Timer 13 Hardware Run Input T2EX_3 Timer 2 External Trigger Input T2_1 Timer 2 Input EXINT0_3 External Interrupt Input 0 AN0 Analog Input 0 / Out of range comparator channel 0 |
| P2.1 | 6/5 | | Hi-Z | CCPOS1_1 CCU6 Hall Input 1 RXD_3 UART Receive Input MTSR_4 Slave Receive Input T0_1 Timer 0 Input EXINT1_1 External Interrupt Input 1 AN1 Analog Input 1 / Out of range comparator channel 1 |
| P2.2 | 5/4 | | Hi-Z | CCPOS2_1 CCU6 Hall Input 2 T12HR_3 CCU6 Timer 12 Hardware Run Input T13HR_3 CCU6 Timer 13 Hardware Run Input SCK_1 SSC Clock Input/Output T1_1 Timer 1 Input EXINT2 External Interrupt Input 2 AN2 Analog Input 2 / Out of range comparator channel 2 |

Table 3 Pin Definitions and Functions for XC822/824

| Symbol | Pin Number DSO20/ TSSOP16 | Type | Reset State | Function |
|--|---------------------------------|------|-------------|---|
| P2.3 | 4/3 | | Hi-Z | CCPOS0_2 CCU6 Hall Input 0 CTRAP_2 CCU6 Trap Input T2_2 Timer 2 Input EXINT3 External Interrupt Input 3 AN3 Analog Input 3 / Out of range comparator channel 3 |
| V _{DDP} | 12/9 | – | | I/O Port Supply (2.5 V - 5.5 V) |
| V _{DDC} | 14/11 | – | | Core Supply Output (2.5 V) |
| V _{SSP} / V _{SSC} | 13/10 | – | | I/O Port Ground/ Core Supply Ground |

2.5 Memory Organization

The XC822/824 CPU operates in the following five address spaces:

- 8 Kbytes of Boot ROM, Library ROM and User routines
- 256 bytes of internal RAM
- 256 bytes of XRAM
(XRAM can be read/written as program memory or external data memory)
- A 128-byte Special Function Register area
- 2/4 Kbytes of Flash

Figure 6 illustrates the memory address spaces of the 2 Kbyte Flash devices. There are two 1-Kbyte sectors in this device. **Figure 7** illustrates the memory address spaces of the 4 Kbyte Flash devices. This device has two 1-Kbyte sectors, two 512-byte sectors, two 256-byte sectors and four 128-byte sectors. **Figure 8** shows the Flash sectorization for 2 Kbyte and 4 Kbyte Flash devices.

General Device Information

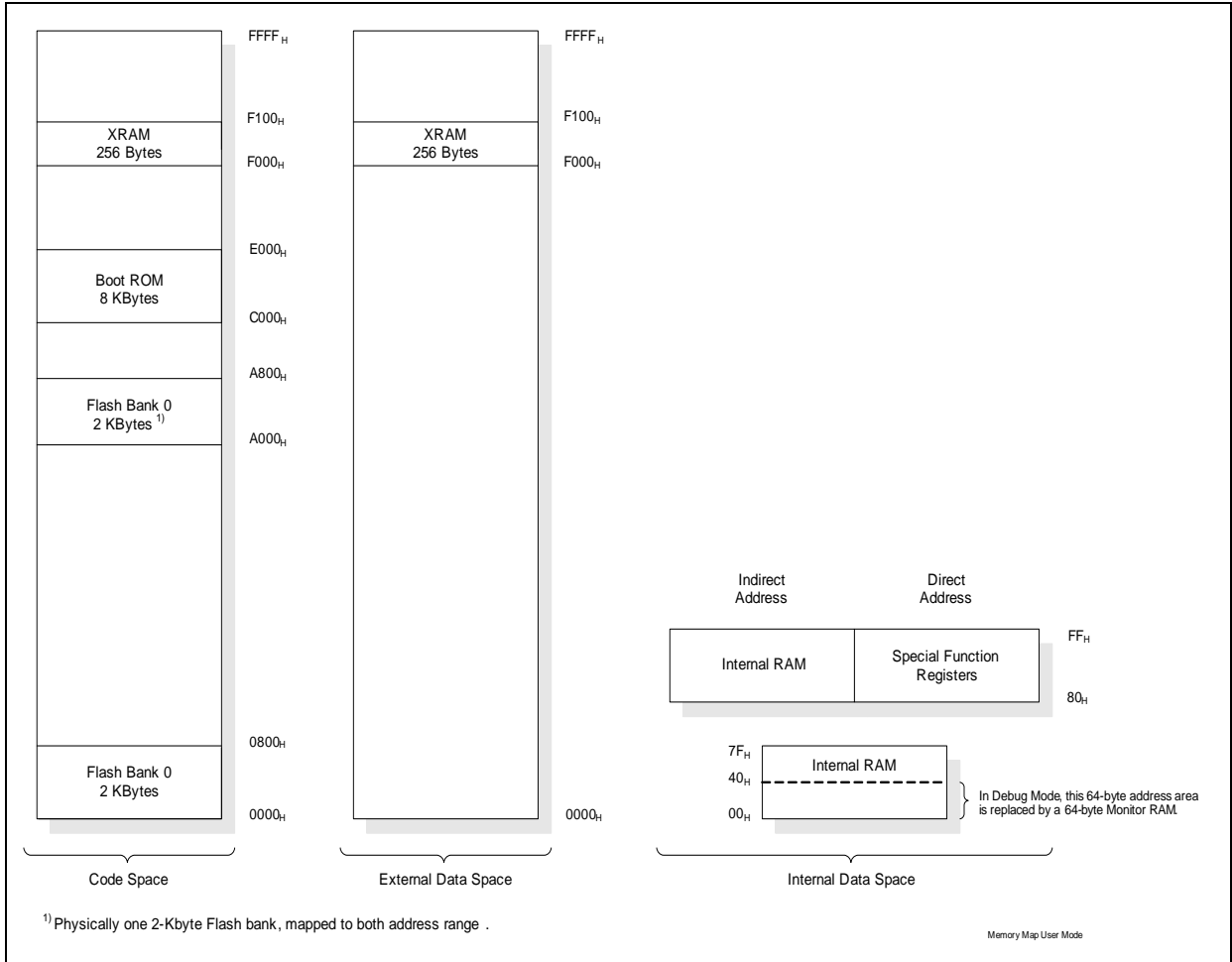


Figure 6 Memory Map of XC822/824 with 2 Kbytes of Flash memory

General Device Information

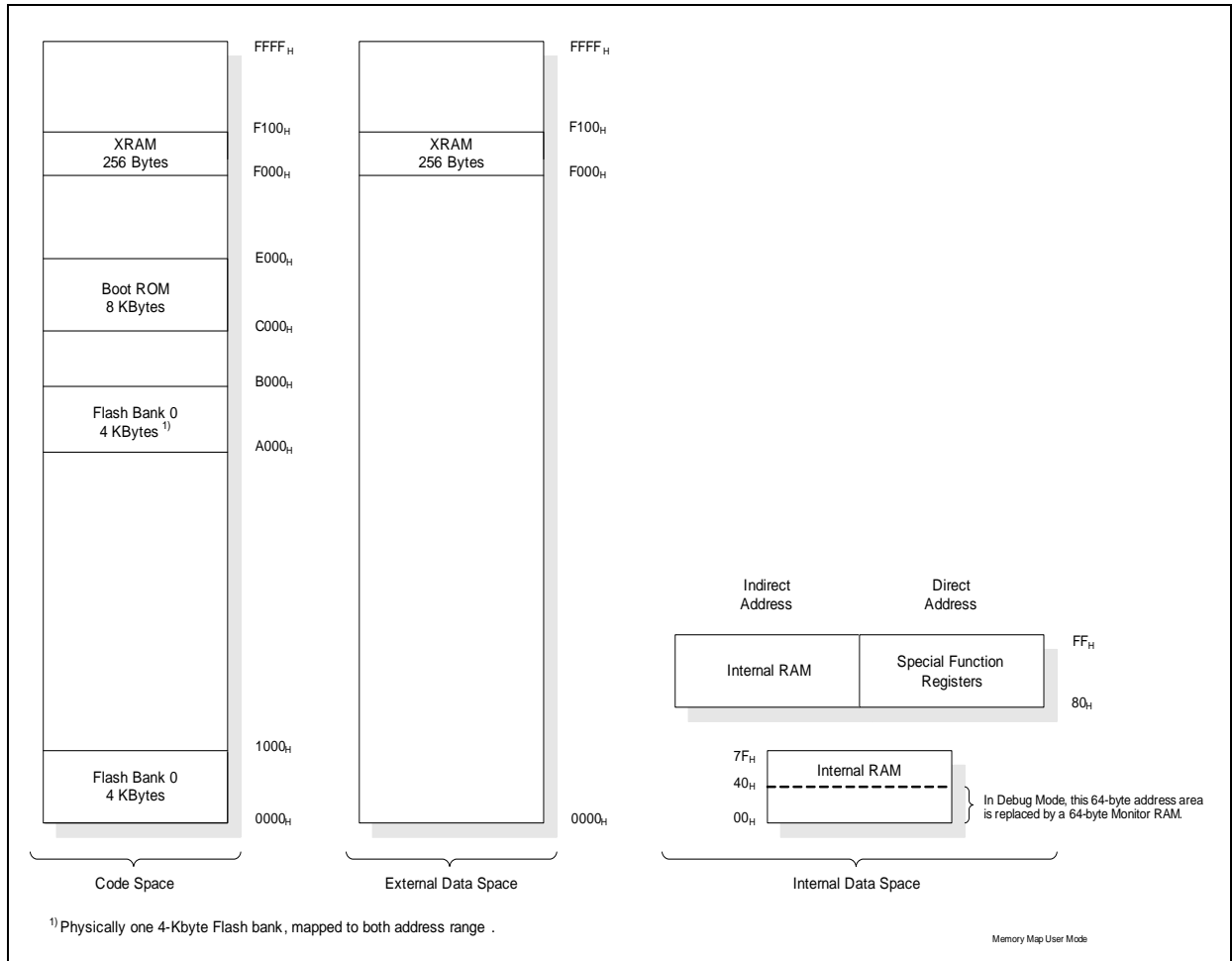


Figure 7 Memory Map of XC822/824 with 4 Kbytes of Flash memory

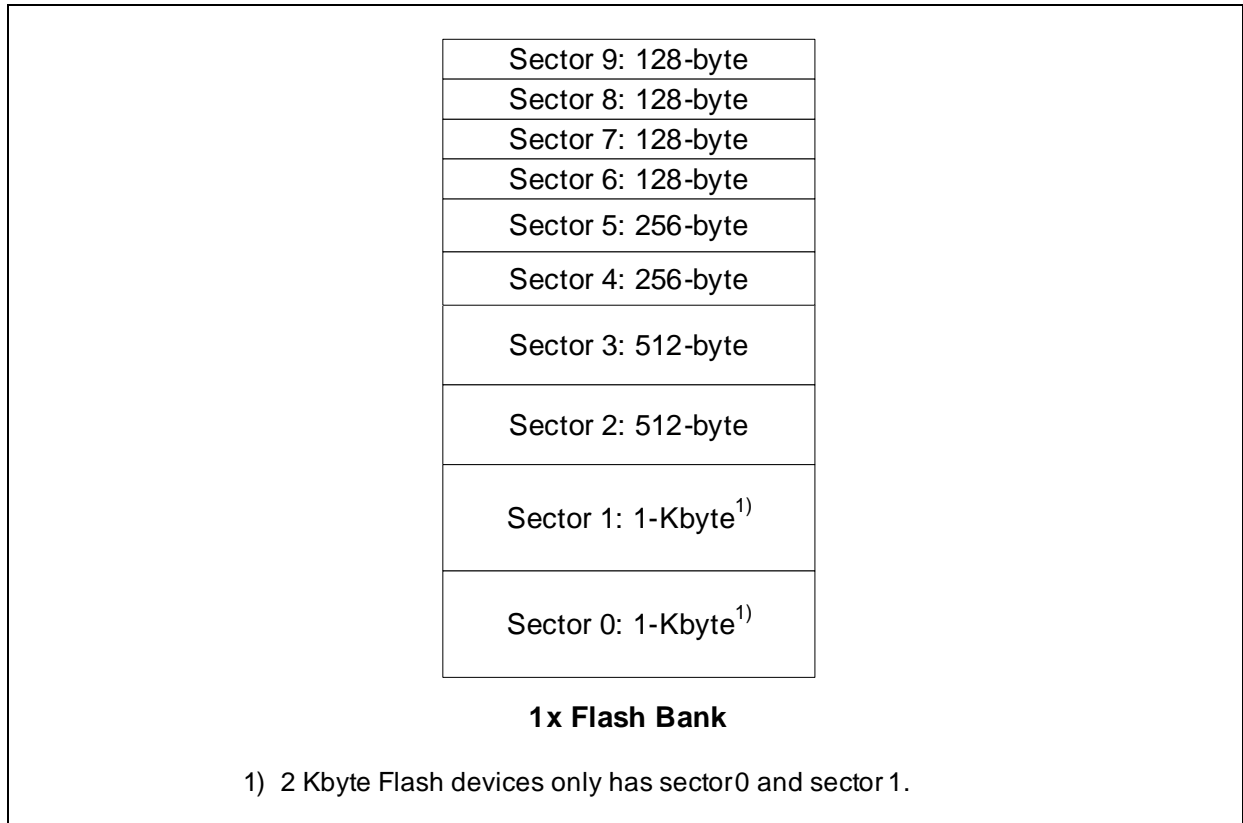


Figure 8 Flash Bank Sectorization

2.6 JTAG ID

JTAG ID register is a read-only register located inside the JTAG module, and is used to recognize the device(s) connected to the JTAG interface. Its content is shifted out when INSTRUCTION register contains the IDCODE command (opcode 04_H), and the same is also true immediately after reset.

The JTAG ID register contents for the XC822/824 Flash devices are given in [Table 4](#).

Table 4 JTAG ID Summary

| Device Type | Device Name | JTAG ID |
|-------------|-------------|------------------------|
| Flash | XC822/824* | 101B C083 _H |

Note: The asterisk () above denotes all possible device configurations.*

2.7 Chip Identification Number

The XC822/824 identity (ID) register is located at Page 1 of address B3_H. The value of ID register is 51_H. However, for easy identification of product variants, the Chip Identification Number, which is a unique number assigned to each product variant, is available. The differentiation is based on the product and variant type information.

Two methods are provided to read a device's Chip Identification number:

- In-application subroutine, GET_CHIP_INFO
- Boot-loader (BSL) mode A

Table 5 lists the Chip Identification numbers of XC822/824 device variants.

Table 5 Chip Identification Number

| Product Variant | Chip Identification Number |
|-----------------|----------------------------|
| XC822T-0FR | 51080343 _H |
| XC822MT-0FR | 51080303 _H |
| XC822-1FR | 51080163 _H |
| XC822T-1FR | 51080143 _H |
| XC822M-1FR | 51080123 _H |
| XC822MT-1FR | 51080103 _H |
| XC824M-1FG | 51080122 _H |
| XC824MT-1FG | 51080102 _H |

3 Electrical Parameters

Chapter 3 provides the characteristics of the electrical parameters which are implementation-specific for the XC822/824.

3.1 General Parameters

The general parameters are described here to aid the users in interpreting the parameters mainly in **Section 3.2** and **Section 3.3**.

3.1.1 Parameter Interpretation

The parameters listed in this section represent partly the characteristics of the XC822/824 and partly its requirements on the system. To aid interpreting the parameters easily when evaluating them for a design, they are indicated by the abbreviations in the "Symbol" column:

- **CC**
 - These parameters indicate **C**ontroller **C**haracteristics, which are distinctive features of the XC822/824 and must be regarded for a system design.
- **SR**
 - These parameters indicate **S**ystem **R**equirements, which must be provided by the microcontroller system in which the XC822/824 is designed in.

3.1.2 Absolute Maximum Rating

Maximum ratings are the extreme limits to which the XC822/824 can be subjected to without permanent damage.

Table 6 Absolute Maximum Rating Parameters

| Parameter | Symbol | Limit Values | | Unit | Notes |
|--|------------------|--------------|------|------|------------|
| | | Min. | Max. | | |
| Ambient temperature | T_A | -40 | 125 | °C | under bias |
| Storage temperature | T_{ST} | -65 | 150 | °C | – |
| Junction temperature | T_J | -40 | 150 | °C | under bias |
| Voltage on power supply pin with respect to V_{SS} | V_{DDP} | -0.5 | 6 | V | |
| Input current on any pin during overload condition | I_{IN} | -10 | 10 | mA | |
| Absolute sum of all input currents during overload condition | $\Sigma I_{IN} $ | – | 50 | mA | |

Note: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. During absolute maximum rating overload conditions ($V_{IN} > V_{DDP}$ or $V_{IN} < V_{SS}$) the voltage on V_{DDP} pin with respect to ground (V_{SS}) must not exceed the values defined by the absolute maximum ratings.

3.1.3 Operating Condition

The following operating conditions must not be exceeded in order to ensure correct operation of the XC822/824. All parameters mentioned in the following tables refer to these operating conditions, unless otherwise noted.

Table 7 Operating Condition Parameters

| Parameter | Symbol | Limit Values | | Unit | Notes/ Conditions |
|------------------------------|------------|--------------|------|------|----------------------|
| | | Min. | Max. | | |
| Digital power supply voltage | V_{DDP} | 3.0 | 5.5 | V | |
| | | 2.5 | 3.0 | V | ¹⁾ |
| CPU Clock Frequency | f_{CCLK} | 22.5 | 25.6 | MHz | typ. 24 MHz |
| | | 7.5 | 8.5 | MHz | typ. 8 MHz |
| Ambient temperature | T_A | -40 | 85 | °C | SAF-XC822/824... |
| | | -40 | 105 | °C | SAX-XC824... |
| | | -40 | 125 | °C | SAK-XC824... |

1) In this voltage range, limited operations are available in active mode. Operations in power save modes are fully supported.

3.2 DC Parameters

The electrical characteristics of the DC Parameters are detailed in this section.

3.2.1 Input/Output Characteristics

Table 8 provides the characteristics of the input/output pins of the XC822/XC824.

Table 8 Input/Output Characteristics of XC822/XC824 (Operating Conditions apply)

| Parameter | Symbol | | Limit Values | | Unit | Test Conditions |
|----------------------------------|------------|----|-----------------------|----------------------|---------------|--|
| | | | Min. | Max. | | |
| Output low voltage on port pins | V_{OLP} | CC | – | 1.0 | V | $I_{OL} = 25 \text{ mA}$ (5 V) $I_{OL} = 13 \text{ mA}$ (3.3 V) |
| | | | – | 0.4 | V | $I_{OL} = 10 \text{ mA}$ (5 V) $I_{OL} = 5 \text{ mA}$ (3.3 V) |
| Output high voltage on port pins | V_{OHP} | CC | $V_{DDP} - 1.0$ | – | V | $I_{OH} = -15 \text{ mA}$ (5 V) $I_{OH} = -8 \text{ mA}$ (3.3 V) |
| | | | $V_{DDP} - 0.4$ | – | V | $I_{OH} = -5 \text{ mA}$ (5 V) $I_{OH} = -2.5 \text{ mA}$ (3.3 V) |
| Input low voltage on port pins | V_{ILP} | SR | – | $0.3 \times V_{DDP}$ | V | CMOS Mode |
| Input high voltage on port pins | V_{IHP} | SR | $0.7 \times V_{DDP}$ | – | V | CMOS Mode |
| Input Hysteresis ¹⁾ | <i>HYS</i> | CC | $0.08 \times V_{DDP}$ | – | V | CMOS Mode (5 V) |
| | | | $0.03 \times V_{DDP}$ | – | V | CMOS Mode (3.3 V) |
| | | | $0.01 \times V_{DDP}$ | – | V | CMOS Mode (2.5 V) |
| Pull-up current on port pins | I_{PUP} | CC | – | -20 | μA | $V_{IH,min}$ (5 V) |
| | | | -150 | – | μA | $V_{IL,max}$ (5 V) |
| | | | – | -5 | μA | $V_{IH,min}$ (3.3 V) |
| | | | -100 | – | μA | $V_{IL,max}$ (3.3 V) |

Electrical Parameters
Table 8 Input/Output Characteristics of XC822/XC824 (Operating Conditions apply) (cont'd)

| Parameter | Symbol | | Limit Values | | Unit | Test Conditions |
|---|------------------|----|--------------|------|---------------|--|
| | | | Min. | Max. | | |
| Pull-down current on port pins | I_{PDP} | CC | – | 20 | μA | $V_{IL,max}$ (5 V) |
| | | | 150 | – | μA | $V_{IH,min}$ (5 V) |
| | | | – | 5 | μA | $V_{IL,max}$ (3.3 V) |
| | | | 100 | – | μA | $V_{IH,min}$ (3.3 V) |
| Input leakage current on port pins ²⁾ | I_{OZP} | CC | -1 | 1 | μA | $0 < V_{IN} < V_{DDP}$, $T_A \leq 125\text{ }^\circ\text{C}$ |
| Overload current on any pin | I_{OVP} | SR | -5 | 5 | mA | ³⁾ |
| Absolute sum of overload currents | $\sum I_{OVP} $ | SR | – | 25 | mA | ³⁾ |
| Voltage on any pin during V_{DDP} power off | V_{PO} | SR | – | 0.3 | V | ⁴⁾ |
| Maximum current per pin (excluding V_{DDP} and V_{SS}) | I_M | SR | -15 | 25 | mA | – |
| Maximum current into V_{DDP} | I_{MVDDP} | SR | – | 80 | mA | ³⁾ |
| Maximum current out of V_{SS} | I_{MVSS} | SR | – | 80 | mA | ³⁾ |

- 1) Not subjected to production test, verified by design/characterization. Hysteresis is implemented to avoid meta stable states and switching due to internal ground bounce. It cannot be guaranteed that it suppresses switching due to external system noise.
- 2) An additional error current (I_{INJ}) will flow if an overload current flows through an adjacent pin.
- 3) Not subjected to production test, verified by design/characterization.
- 4) Not subjected to production test, verified by design/characterization. However, for applications with strict low power-down current requirements, it is mandatory that no active voltage source is supplied at any GPIO pin when V_{DDP} is powered off.

3.2.2 Supply Threshold Characteristics

Table 9 provides the characteristics of the supply threshold in the XC822/824.

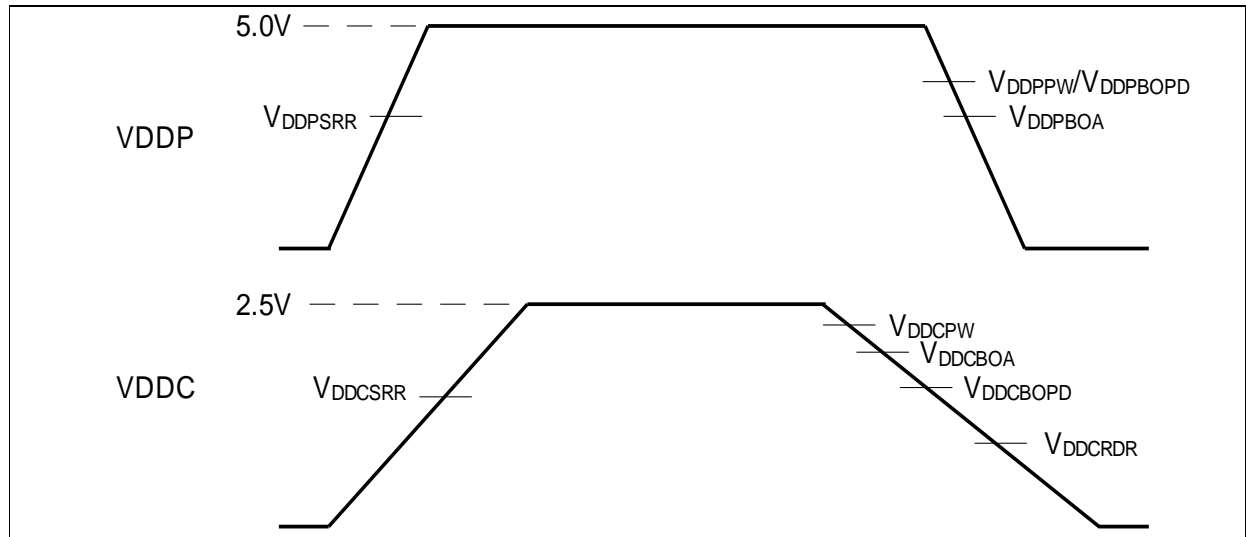


Figure 9 Supply Threshold Parameters

Table 9 Supply Threshold Parameters (Operating Conditions apply)

| Parameters | Symbol | | Limit Values | | | Unit |
|---|---------------|----|--------------|------|------|------|
| | | | Min. | Typ. | Max. | |
| V_{DDP} prewarning voltage ¹⁾²⁾ | V_{DDPPW} | CC | 3.0 | 3.6 | 4.5 | V |
| V_{DDP} brownout voltage in active mode ³⁾²⁾ | V_{DDPBOA} | CC | 2.65 | 2.75 | 2.87 | V |
| V_{DDP} brownout voltage in power down mode ²⁾³⁾ | $V_{DDPBOPD}$ | CC | 3.0 | 3.6 | 4.5 | V |
| V_{DDP} system reset release voltage ²⁾⁴⁾ | V_{DDPSRR} | CC | 2.7 | 2.8 | 2.92 | V |
| V_{DDC} prewarning voltage ²⁾⁵⁾ | V_{DDCPW} | CC | 2.3 | 2.4 | 2.48 | V |
| V_{DDC} brownout voltage in active mode ²⁾ | V_{DDCBOA} | CC | 2.25 | 2.3 | 2.42 | V |
| V_{DDC} brownout voltage in power down mode ²⁾ | $V_{DDCBOPD}$ | CC | 1.35 | 1.5 | 1.95 | V |
| V_{DDC} system reset release voltage ²⁾⁴⁾ | V_{DDCSRR} | CC | 2.28 | 2.3 | 2.47 | V |
| RAM data retention voltage | V_{DDCRDR} | CC | 1.1 | – | – | V |

1) Detection is enabled via SDCON register in active mode. It is automatically disabled in power down mode. Detection should be disabled for V_{DDP} less than maximum of V_{DDPPW} .

2) This parameter has a hysteresis of 50 mV.

3) Detection is enabled via SDCON register. Detection must be disabled for application with V_{DDP} less than the specified values.

4) V_{DDPSRR} and V_{DDCSRR} must be met before the system reset is released.

5) Detection is enabled via SDCON register in active mode. It is automatically disabled in power down mode.

3.2.3 ADC Characteristics

The values in [Table 10](#) are given for an analog power supply of 5.0 V. The ADC can be used with an analog power supply down to 3 V. But in this case, analog parameters may show a reduced performances. In the reduced voltage mode ($2.5\text{ V} < V_{DDP} < 3\text{ V}$), the ADC is not recommended to be used.

Table 10 ADC Characteristics (Operating Conditions apply; $V_{DDP} = 5\text{ V}$)

| Parameter | Symbol | | Limit Values | | | Unit | Test Conditions / Remarks |
|-----------------------------------|---------------|----|-------------------------------------|-----------|------------|---------------|--|
| | | | Min. | Typ. | Max. | | |
| Analog reference voltage | V_{AREF} | | – | V_{DDP} | – | V | Connect internally to V_{DDP} |
| Analog reference ground | V_{AGND} | | – | V_{SSP} | – | V | Connect internally to V_{SSP} |
| Alternate analog reference ground | $V_{AGNDALT}$ | SR | $V_{SSP} - 0.1$ | – | $2.5^1)$ | V | Connect to AN0 in differential mode, See Figure 10 . |
| Internal voltage reference | V_{INTREF} | SR | 1.19 | 1.23 | 1.28 | V | ³⁾ |
| Analog input voltage range | V_{AIN} | SR | V_{AGND} | – | V_{AREF} | V | – |
| ADC clock | f_{ADCI} | | 8 | – | 16 | MHz | internal analog clock |
| Sample time | t_S | CC | $(2 + INPCR0.STC) \times t_{ADCI}$ | | | μs | – |
| Conversion time | t_C | CC | See Section 3.2.3.1 | | | μs | – |
| Total unadjusted error | $TUE^2)$ | CC | – | – | ± 1 | LSB8 | 8-bit conversion with internal reference ³⁾ |
| | | | – | – | +4/-1 | LSB10 | 10-bit conversion with internal reference ³⁾⁴⁾ |
| | | | – | – | +14/-2 | LSB12 | 12-bit conversion using the Low Pass Filter ³⁾ |
| Differential Nonlinearity | EA_{DNL} | CC | – | – | +1.5/-1 | LSB | 10-bit conversion ³⁾ |

Electrical Parameters
Table 10 ADC Characteristics (Operating Conditions apply; $V_{DDP} = 5\text{ V}$)

| Parameter | Symbol | | Limit Values | | | Unit | Test Conditions / Remarks |
|---|-------------|----|--------------|------|-----------|------------|---------------------------------|
| | | | Min. | Typ. | Max. | | |
| Integral Nonlinearity | EA_{INL} | CC | – | – | ± 1.5 | LSB | 10-bit conversion ³⁾ |
| Offset | EA_{OFF} | CC | – | +4 | – | LSB | 10-bit conversion ³⁾ |
| Gain | EA_{GAIN} | CC | – | -4 | – | LSB | 10-bit conversion ³⁾ |
| Switched capacitance at an analog input | C_{AINSW} | CC | – | 2 | 3 | pF | 3)5) |
| Total capacitance at an analog input | C_{AINT} | CC | – | – | 12 | pF | 3)5) |
| Input resistance of an analog input | R_{AIN} | CC | – | 1.5 | 2 | k Ω | 3) |

1) 1.2 V at $V_{DDP} = 3.0\text{ V}$.

2) TUE is tested at $V_{AREF} = V_{DDP} = 5.0\text{ V}$ and CPU clock ($f_{SCLK, CCLK}$) = 8 MHz.

3) Not subject to production test, verified by design/characterization.

4) If a reduced positive reference voltage is used, TUE will increase. If the positive reference is reduced by a factor of K, the TUE will increased by 1/K. Example:K = 0.8, 1/K = 1.25; 1.25 X TUE = 2.5 LSB10.

5) The sampling capacity of the conversion C-Network is pre-charged to $V_{AREF}/2$ before connecting the input to the C-Network. Because of the parasitic elements, the voltage measured at ANx is lower than $V_{AREF}/2$.

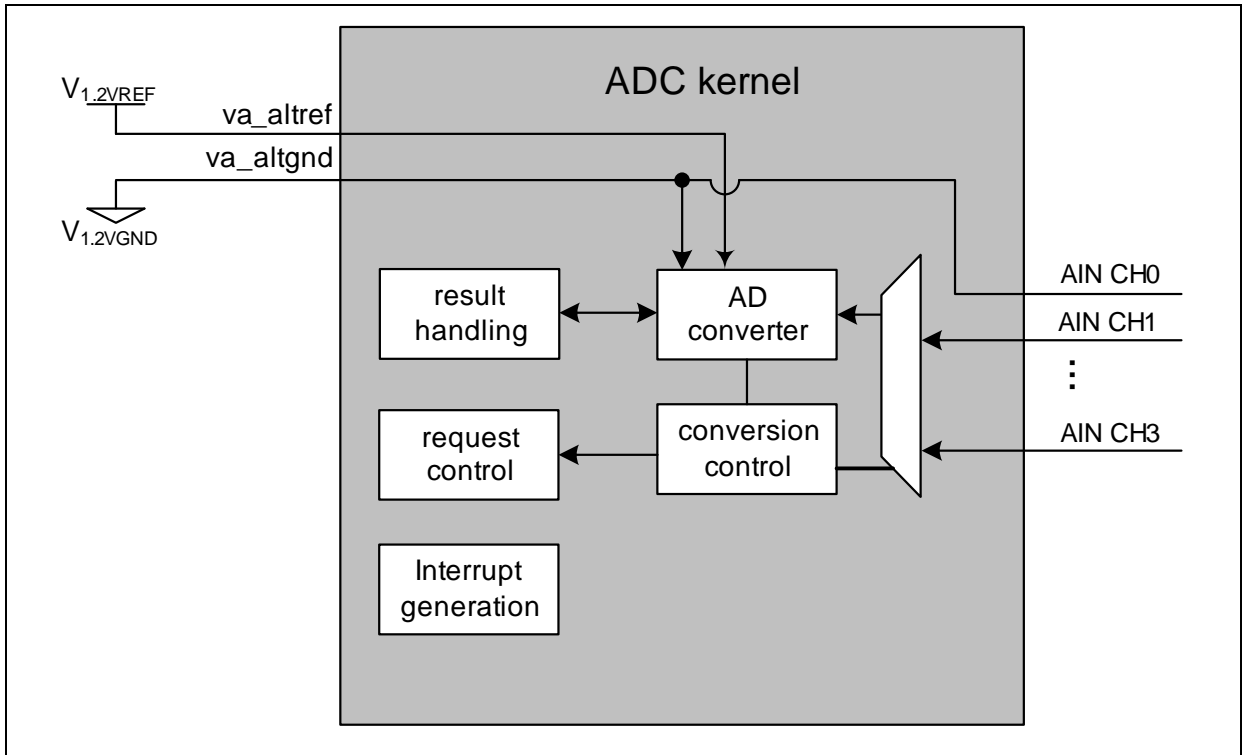


Figure 10 Differential like measurement with internal 1.2V voltage reference, and CH0 gnd.

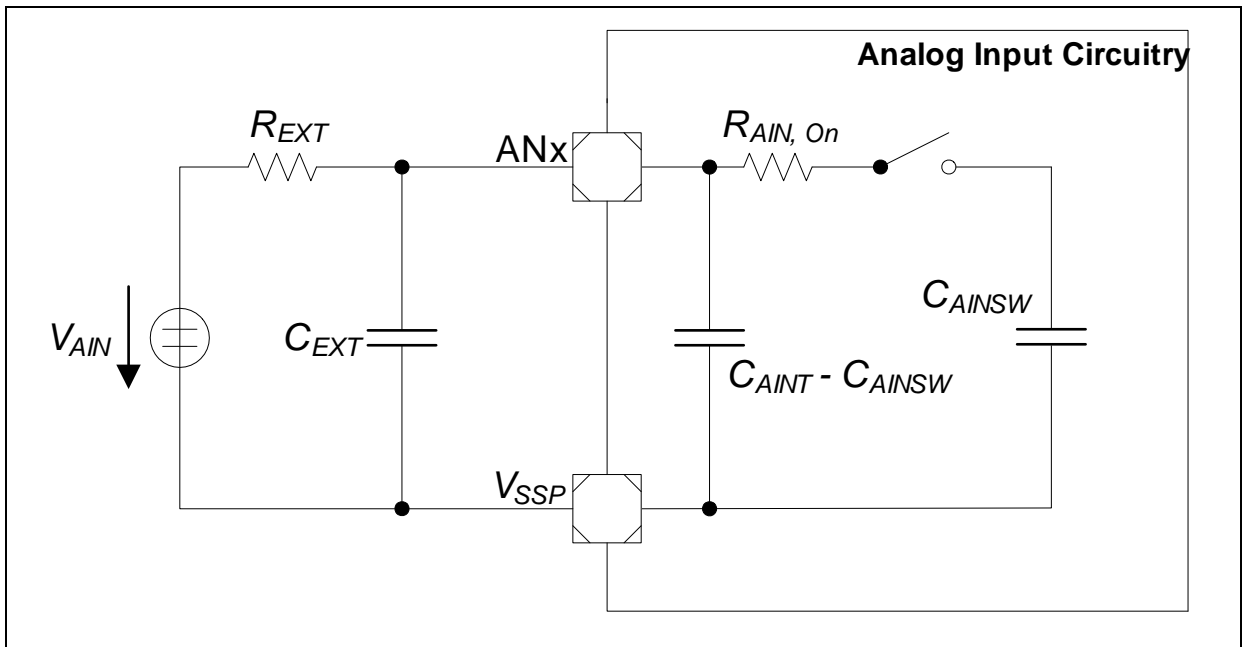


Figure 11 ADC Input Circuits

3.2.3.1 ADC Conversion Timing

Conversion time, $t_C = t_{ADC} \times (1 + r \times (3 + n + STC))$, where

- $r = CTC + 3$,
- $CTC =$ Conversion Time Control (GLOBCTR.CTC),
- $STC =$ Sample Time Control (INPCR0.STC),
- $n = 8$ or 10 (for 8-bit and 10-bit conversion respectively),
- $t_{ADC} = 1 / f_{ADC}$

3.2.3.2 Out of Range Comparator Characteristics

Table 11 below shows the Out of Range Comparator characteristics.

Table 11 Out of Range Comparator Characteristics (Operating Conditions apply)

| Parameter | Symbol | | Limit Values | | | Unit | Remarks |
|-----------------------|----------------|----|--------------|------|------|------|---|
| | | | Min. | Typ. | Max. | | |
| DC Switching Level | $V_{SenseDC}$ | SR | 60 | 125 | 270 | mV | Above V_{DDP} |
| DC Hysteresis | $V_{SenseHys}$ | CC | 30 | – | – | mV | ¹⁾ |
| Pulse Width | $t_{SensePW}$ | SR | 300 | – | – | ns | $ANx > V_{DDP}$ ¹⁾ |
| Switching Delay | $t_{SenseSD}$ | CC | – | – | 400 | ns | $ANx \geq V_{DDP} + 350$ mV ¹⁾ |
| Pulse Switching Level | $t_{SensePSL}$ | SR | – | 250 | – | mV | @ 300 nsec ¹⁾ |
| | | SR | – | 60 | – | mV | @ 800 usec ¹⁾ |

1) Not subject to production test, verified by design/characterization.

3.2.4 Flash Memory Parameters

The XC822/824 is delivered with all Flash sectors erased (read all zeros).

The data retention time of the XC822/824's Flash memory (i.e. the time after which stored data can still be retrieved) depends on the number of times the Flash memory has been erased and programmed.

Note: Flash memory parameters are not subject to production test but verified by design and/or characterization.

Table 12 Flash Timing Parameters (Operating Conditions apply)

| Parameter | Symbol | CC | Limit Values | | | Unit | Remarks |
|----------------------------------|---------------|----|--------------|------|------|------|--------------------|
| | | | Min. | Typ. | Max. | | |
| Read access time (per byte) | t_{ACC} | CC | – | 125 | – | ns | |
| Programming time (per wordline) | t_{PR} | CC | – | 2.2 | – | ms | |
| Erase time (one or more sectors) | t_{ER} | CC | – | 120 | – | ms | |
| Flash wait states | $N_{WSFLASH}$ | CC | 0 | | | | CPU clock = 8 MHz |
| | | | 1 | | | | CPU clock = 24 MHz |

Table 13 Flash Data Retention and Endurance (Operating Conditions apply)

| Retention | Endurance ¹⁾ | Size | Remarks |
|-----------|-------------------------|----------------|---------|
| 20 years | 1,000 cycles | up to 8 Kbytes | |
| 5 years | 10,000 cycles | 1 Kbyte | |
| 2 years | 70,000 cycles | 512 bytes | |
| 2 years | 100,000 cycles | 128 bytes | |

1) One cycle refers to the programming of all wordlines in a sector and erasing of sector. The Flash endurance data specified in **Table 13** is valid only if the following conditions are fulfilled:

- the maximum number of erase cycles per Flash sector must not exceed 100,000 cycles.
- the maximum number of erase cycles per Flash bank must not exceed 300,000 cycles.
- the maximum number of program cycles per Flash bank must not exceed 2,500,000 cycles.

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Table 14 Emulated Flash Data Retention and Endurance based on EEPROM Emulation ROM Library (Operating Conditions apply)¹⁾

| Retention | Endurance ²⁾ | Emulation Size | Remarks |
|-----------|-------------------------|----------------|---------|
| 2 years | 1,600,000 cycles | 31 bytes | |
| 2 years | 1,400,000 cycles | 62 bytes | |
| 2 years | 1,200,000 cycles | 93 bytes | |
| 2 years | 1,000,000 cycles | 124 bytes | |

1) EEPROM Emulation ROM Library can only be used in the 4 Kbyte Flash variant.

2) These values show the maximum endurance. Maximum endurance is the maximum possible unique data write if each data update is only 31 bytes. Minimum endurance cycle is the maximum possible unique data write if each data update is the same as the emulation size. The minimum endurance cycle can be calculated using the formulae $[(\text{max. endurance}) \cdot (31) / (\text{emulation size})]$.

3.2.5 Power Supply Current

Table 15 provides the characteristics of the power supply current in the XC822/824.

Table 15 Power Consumption Parameters^{1) 2)}(Operating Conditions apply)

| Parameter | Symbol | Limit Values | | Unit | Test Condition |
|-------------------|------------|--------------|------|------|--|
| | | Typ. | Max. | | |
| Active Mode | I_{DDPA} | 21 | 25 | mA | 5 V / 3.3 V ³⁾ |
| | | 14 | 18 | mA | 5 V / 3.3 V ⁴⁾ |
| | | – | 5 | mA | 2.5 V ⁵⁾ |
| Idle Mode | I_{DDPI} | 16 | 20 | mA | 5 V / 3.3 V ⁶⁾ |
| | | – | 5 | mA | 2.5 V ⁵⁾ |
| Power Down Mode 1 | I_{PDP1} | 3 | 5 | μA | $T_A = 25^\circ\text{C}$ ⁷⁾ |
| | | – | 28 | μA | $T_A = 85^\circ\text{C}$ ⁷⁾⁸⁾⁹⁾ |
| Power Down Mode 2 | I_{PDP2} | 5 | 7 | μA | $T_A = 25^\circ\text{C}$ ⁷⁾ |
| | | – | 30 | μA | $T_A = 85^\circ\text{C}$ ⁷⁾⁸⁾ |

- 1) The typical values are measured at $T_A = +25^\circ\text{C}$ and $V_{DDP} = 5\text{ V}$ and 3.3 V .
- 2) The maximum values are measured under worst case conditions ($T_A = +125^\circ\text{C}$ and $V_{DDC} = 5\text{ V}$) unless stated otherwise.
- 3) I_{DDPA} (active mode) is measured with: CPU clock and input clock to all peripherals running at 24 MHz (CLKMODE=0).
- 4) I_{DDPA} (active mode) is measured with: CPU clock and input clock to all peripherals running at 8 MHz (CLKMODE=1).
- 5) This value is based on the maximum load capacity of EVR during $V_{DDP} = 2.5\text{ V}$. Not subject to production test, verified by design/characterisation.
- 6) I_{DDPI} (idle mode) is measured with: CPU clock disabled, watchdog timer disabled, input clock to all peripherals enabled and running at 24 MHz (CLKMODE=0).
- 7) I_{PDP1} and I_{PDP2} is measured at 5 V and 3.3 V with: wake-up port is programmed to be input with either internal pull devices enabled or driven externally to ensure no floating inputs.
- 8) Not subject to production test, verified by design/characterisation.
- 9) I_{PDP1} and I_{PDP2} has a maximum values of 100 uA at $T_A = +125^\circ\text{C}$.

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Table 16 shows the maximum active current within the device in the reduced voltage condition of $2.5\text{ V} < V_{\text{DDP}} < 3.0\text{ V}$. The active current consumption needs to be below the specified values as according to the V_{DDP} voltage. If the conditions are not met, a brownout reset may be triggered.

Table 16 Active Current Consumption in Reduced Voltage Condition

| V_{DDP} | 2.5 V | 2.6 V | 2.7 V | 2.8 V |
|-------------------------------|-------|-------|-------|-------|
| Maximum active current | 7 mA | 13 mA | 20 mA | 25 mA |

Table 17 provides the active current consumption of some modules operating at 8 MHz active mode, 3 V power supply at 25°C . The typical values shown are used as a reference guide for device operating in reduced voltage conditions.

Table 17 Typical Active Current Consumption^{1) 2)}

| Active Current Consumption | Symbol | Limit Values | Unit | Test Condition |
|--------------------------------|----------------------|--------------|---------------|--|
| | | Typ. | | |
| Baseload current ³⁾ | I_{CPUDDC} | 5850 | μA | Modules including Core, memories, UART, T0, T1 and EVR. Disable ADC analog (GLOBCTR.ANON = 0). |
| ADC ⁴⁾ | I_{ADCDDC} | 3390 | μA | Set PMCON1.ADC_DIS to 0 and GLOBECTR.ANON to 1 |
| SSC ⁵⁾ | I_{SSCDDC} | 460 | μA | Set PMCON1.SSC_DIS to 0 |
| CCU6 ⁶⁾ | I_{CCU6DDC} | 3320 | μA | Set PMCON1.CCU_DIS to 0 |
| Timer 2 ⁷⁾ | I_{T2DDC} | 200 | μA | Set PMCON1.T2_DIS to 0 |
| MDU ⁸⁾ | I_{MDUDDC} | 1260 | μA | Set PMCON1.MDU_DIS to 0 |
| LEDTSCU ⁹⁾ | I_{LEDDDC} | 520 | μA | Set PMCON1.LTS_DIS to 0 |
| IIC ¹⁰⁾ | I_{IICDDC} | 580 | μA | Set PMCON1.IIC_DIS to 0 |

1) Modules that are controllable by programming the register PMCON1.

2) Not subject to production test, verified by design/characterisation.

3) Baseload current is measured when the device is running in user mode with an endless loop in the flash memory. All modules in register PMCON1 are disabled.

4) ADC active current is measured with: module enable, ADC analog clock at 8MHz, running in parallel conversion request in autoscan mode for 4 channels

5) SSC active current is measured with: module enabled, running in loop back mode at a baud rate of 1 MBaud

6) CCU6 active current is measured with: module enabled, all timers running in 8 MHz, 6 PWM outputs are generated.

7) Timer 2 active current is measured with: module enabled, timer running in 8 MHz

8) MDU active current is measured with: module enabled, division operation was performed.

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- 9) LEDTSCU active current is measured with: module enabled, counter running in 8 MHz.
- 10) IIC active current is measured with: module enabled, performing a master transmit with the master clock running at 400 KHz.

3.3 AC Parameters

The electrical characteristics of the AC Parameters are detailed in this section.

3.3.1 Testing Waveforms

The testing waveforms for rise/fall time, output delay and output high impedance are shown in [Figure 12](#), [Figure 13](#) and [Figure 14](#).

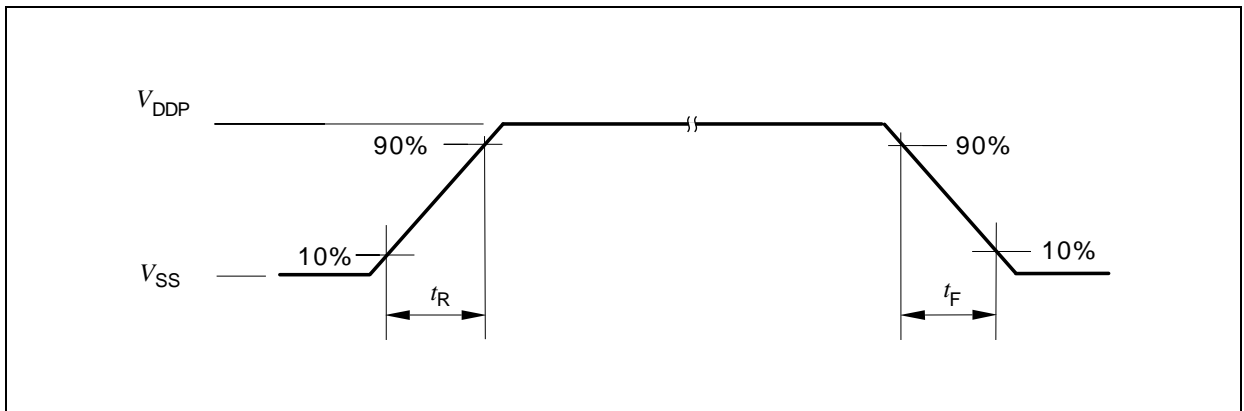


Figure 12 Rise/Fall Time Parameters

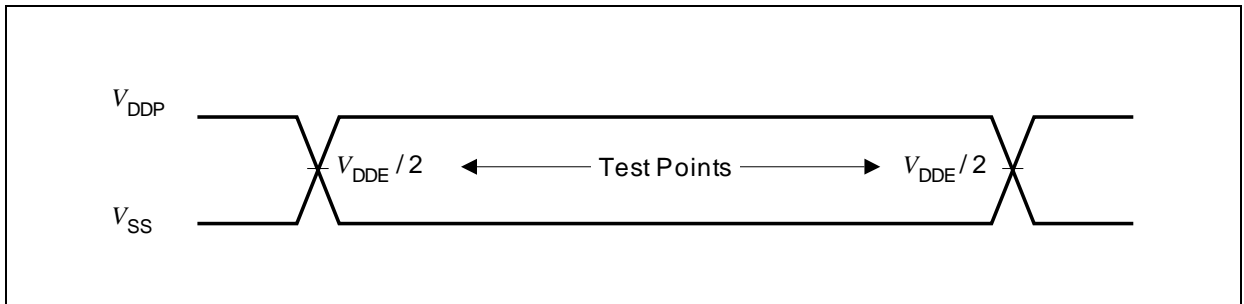


Figure 13 Testing Waveform, Output Delay

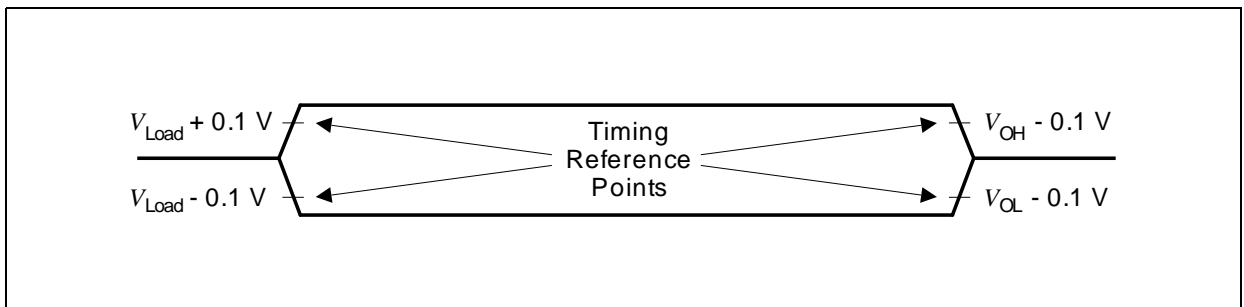


Figure 14 Testing Waveform, Output High Impedance

3.3.2 Output Rise/Fall Times

Table 18 provides the characteristics of the output rise/fall times in the XC822/824.

Table 18 Output Rise/Fall Times Parameters (Operating Conditions apply)

| Parameter | Symbol | Limit Values | | Unit | Test Conditions |
|---|------------|--------------|------|------|---|
| | | Min. | Max. | | |
| Rise/fall times on Standard Pad ¹⁾²⁾ | t_R, t_F | – | 10 | ns | 20 pF ³⁾⁴⁾ (5 V & 3.3 V). |

- 1) Rise/Fall time parameters are taken with 10% - 90% of supply.
- 2) Not all parameters are 100% tested, but are verified by design/characterisation and test correlation.
- 3) Additional rise/fall time valid for $C_L = 20 \text{ pF} - C_L = 100 \text{ pF}$ @ 0.125 ns/pF at 5 V supply voltage.
- 4) Additional rise/fall time valid for $C_L = 20 \text{ pF} - C_L = 100 \text{ pF}$ @ 0.225 ns/pF at 3.3 V supply voltage.

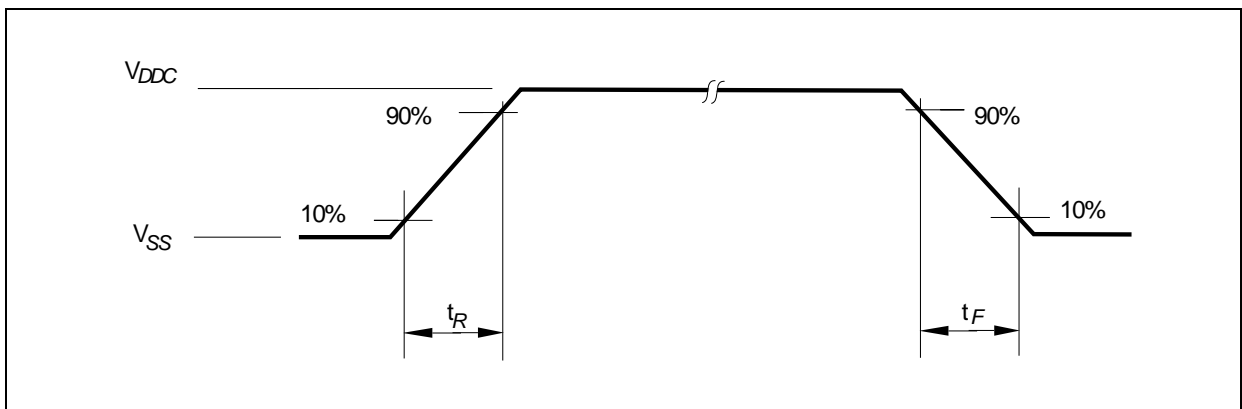


Figure 15 Rise/Fall Times Parameters

3.3.3 Oscillator Timing and Wake-up Timing

Table 19 provides the characteristics of the power-on reset, PLL and Wake-up timings in the XC822/824.

Table 19 Power-On Reset Wake-up Timing¹⁾ (Operating Conditions apply)

| Parameter | Symbol | Limit Values | | | Unit | Test Conditions |
|---------------------------------|--------------------------|--------------|------|------|---------------|-----------------|
| | | Min. | Typ. | Max. | | |
| 48 MHz Oscillator start-up time | $t_{48\text{MOSCST}}$ CC | – | – | 13 | μs | |
| 75 KHz Oscillator start-up time | $t_{75\text{KOSCST}}$ CC | – | – | 800 | μs | |
| Flash initialization time | t_{FINT} CC | – | 160 | – | μs | |

1) Not subject to production test, verified by design/characterisation.

3.3.4 On-Chip Oscillator Characteristics

Table 20 provides the characteristics of the 48 MHz oscillator in the XC822/824.

Table 20 48 MHz Oscillator Characteristics (Operating Conditions apply)

| Parameter | Symbol | Limit Values | | | Unit | Test Conditions |
|--|---------------------------|--------------|------|-------|------|---|
| | | Min. | Typ. | Max. | | |
| Nominal frequency | f_{NOM} CC | -0.5 % | 48 | +0.5% | MHz | under nominal conditions ¹⁾ after trimming |
| Long term frequency deviation | Δf_{LT} CC | -2.0 | – | 3.0 | % | with respect to f_{NOM} , over lifetime and temperature (0 °C to 85 °C) |
| | | -4.5 | – | 4.5 | % | with respect to f_{NOM} , over lifetime and temperature (-40 °C to 125 °C) |
| Short term frequency deviation (over core supply voltage ²⁾) | Δf_{ST} CC | -1 | – | 1 | % | with respect to f_{NOM} , within one LIN message (< 10 ms ... 100 ms) |

1) Nominal condition: $V_{\text{DCC}} = 2.5 \text{ V}$, $T_{\text{A}} = +25^{\circ}\text{C}$.

2) Core voltage supply, $V_{\text{DCC}} = 2.5 \text{ V} \pm 7.5\%$.

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Table 21 provides the characteristics of the 75 kHz oscillator in the XC822/824.

Table 21 75 kHz Oscillator Characteristics (Operating Conditions apply)

| Parameter | Symbol | | Limit Values | | | Unit | Test Conditions |
|--------------------------------|------------------------|----|--------------|------|------|------|---|
| | | | Min. | Typ. | Max. | | |
| Nominal frequency | f_{NOM} | CC | -1% | 75 | +1% | KHz | under nominal conditions ¹⁾ after trimming |
| Long term frequency deviation | Δf_{LT} | CC | -4.5 | – | 4.5 | % | with respect to f_{NOM} , over lifetime and temperature (-40 °C to 125 °C) |
| Short term frequency deviation | Δf_{ST} | CC | -1.5 | – | 1.5 | % | with respect to f_{NOM} , over core supply voltage of 2.5 V \pm 7.5% |

1) Nominal condition: $V_{\text{DDC}} = 2.5 \text{ V}$, $T_{\text{A}} = +25^{\circ}\text{C}$.

3.3.5 SSC Timing

3.3.5.1 SSC Master Mode Timing

Table 22 provides the SSC master mode timing in the XC822/824.

Table 22 SSC Master Mode Timing¹⁾ (Operating Conditions apply; CL = 50 pF)

| Parameter | Symbol | | Limit Values | | Unit |
|----------------------|--------|----|--------------------|------|------|
| | | | Min. | Max. | |
| SCLK clock period | t_0 | CC | $2 * T_{SSC}^{2)}$ | – | ns |
| MISR delay from SCLK | t_1 | CC | 0 | 6 | ns |
| MRST setup to SCLK | t_2 | SR | 20 | – | ns |
| MRST hold from SCLK | t_3 | SR | 0 | – | ns |

1) Not subject to production test, verified by design/characterisation.

2) $T_{SSCmin} = T_{CPU} = 1/f_{CPU}$. When $f_{CPU} = 24$ MHz, $t_0 = 83.3$ ns. T_{CPU} is the CPU clock period.

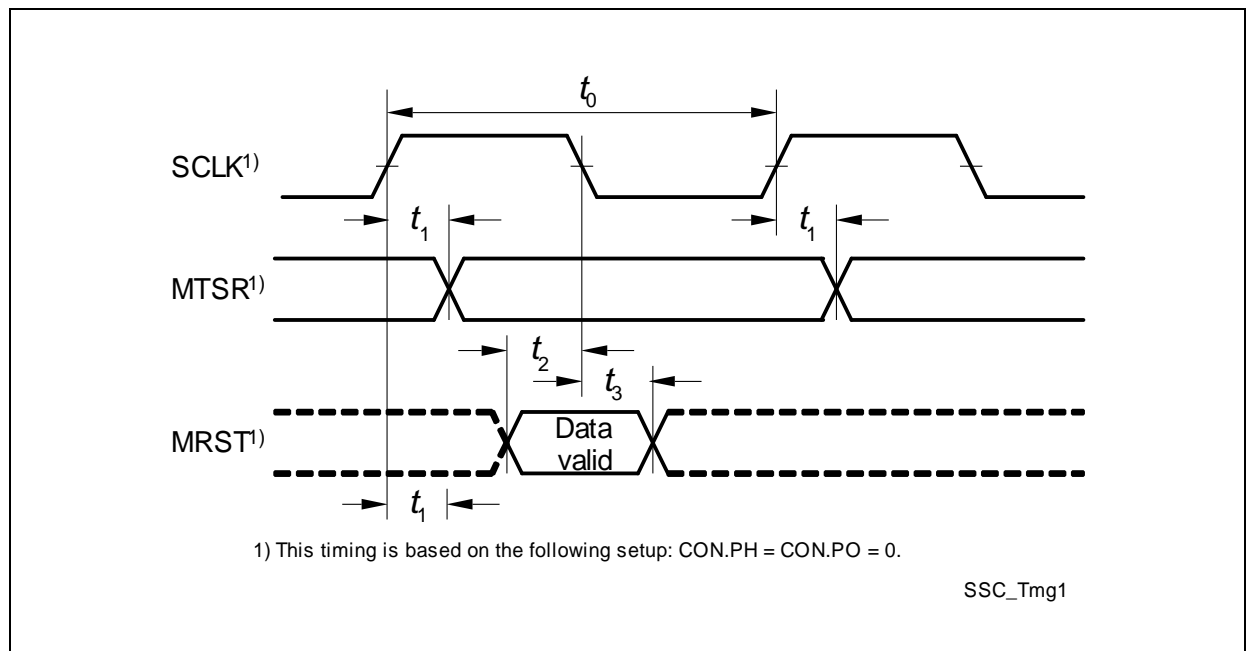


Figure 16 SSC Master Mode Timing

3.3.5.2 SSC Slave Mode Timing

Table 23 provides the SSC slave mode timing in the XC822/824.

Table 23 SSC Slave Mode Timing¹⁾ (Operating Conditions apply; CL = 50 pF)

| Parameter | Symbol | Limit Values | | Unit |
|----------------------|----------|--------------------|------|------|
| | | Min. | Max. | |
| SCLK clock period | t_0 SR | $4 * T_{SSC}^{2)}$ | – | ns |
| MRST delay from SCLK | t_1 CC | 0 | 20 | ns |
| MTSR setup to SCLK | t_2 SR | 46 | – | ns |
| MTSR hold from SCLK | t_3 SR | 0 | – | ns |

- 1) Not subject to production test, verified by design/characterisation.
- 2) $T_{SSCmin} = T_{CPU} = 1/f_{CPU}$. When $f_{CPU} = 24$ MHz, $t_0 = 166.7$ ns. T_{CPU} is the CPU clock period.

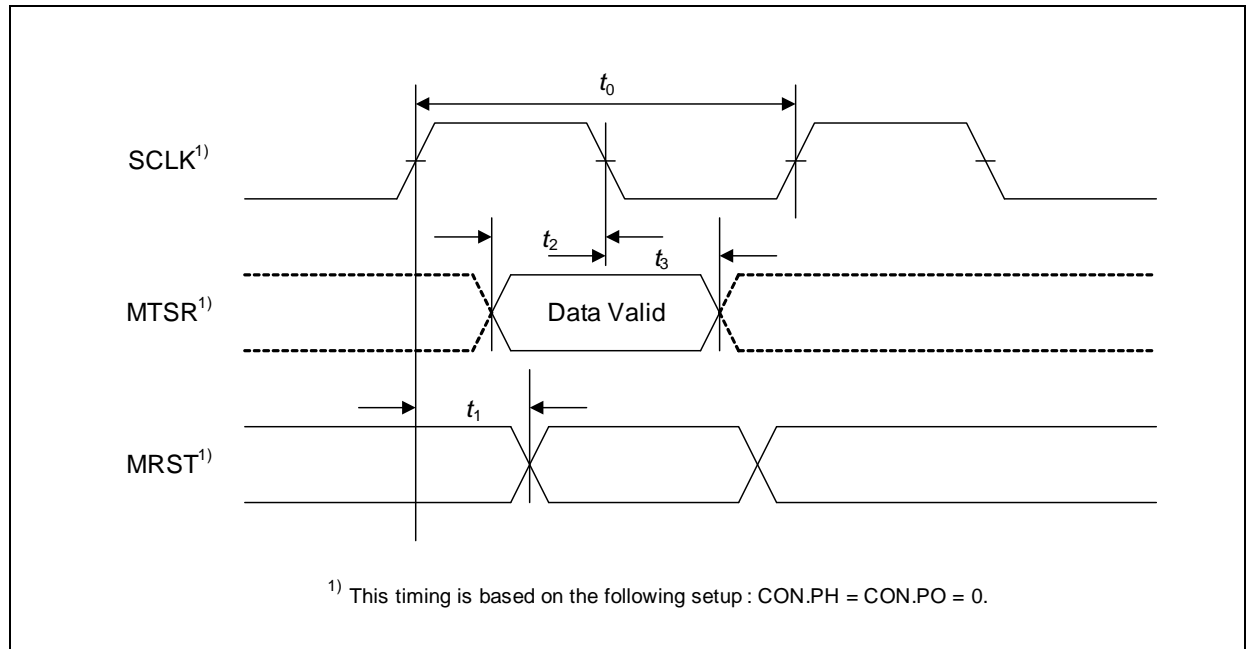


Figure 17 SSC Slave Mode Timing

3.3.6 SPD Timing

The SPD interface will work with standard SPD tools having a sample/output clock frequency deviation of +/- 5% or less. For further details please refer to application note AP24004 in section SPD Timing Requirements.

Note: These parameters are no subject to product test but verified by design and/or characterization.

Note: Operating Conditions apply.

4 Package and Quality Declaration

Chapter 4 provides the information of the XC822/824 package and reliability section.

4.1 Package Parameters

Table 24 provides the thermal characteristics of the packages used in XC822 and XC824 respectively.

Table 24 Thermal Characteristics of the Packages

| Parameter | Symbol | | Limit Values | | Unit | Package Types |
|--|-----------|----|--------------|-------|------|---------------|
| | | | Min. | Max. | | |
| Thermal resistance junction case ¹⁾ | R_{TJC} | CC | - | 36.2 | K/W | PG-TSSOP-16-1 |
| | | | - | 34.3 | | K/W |
| Thermal resistance junction lead ¹⁾ | R_{TJL} | CC | - | 356.6 | K/W | PG-TSSOP-16-1 |
| | | | - | 36.2 | | K/W |

1) The thermal resistances between the case and the ambient (R_{TCA}), the lead and the ambient (R_{TLA}) are to be combined with the thermal resistances between the junction and the case (R_{TJC}), the junction and the lead (R_{TJL}) given above, in order to calculate the total thermal resistance between the junction and the ambient (R_{TJA}). The thermal resistances between the case and the ambient (R_{TCA}), the lead and the ambient (R_{TLA}) depend on the external system (PCB, case) characteristics, and are under user responsibility.

The junction temperature can be calculated using the following equation: $T_J = T_A + R_{TJA} \times P_D$, where the R_{TJA} is the total thermal resistance between the junction and the ambient. This total junction ambient resistance R_{TJA} can be obtained from the upper four partial thermal resistances, by

- a) simply adding only the two thermal resistances (junction lead and lead ambient), or
- b) by taking all four resistances into account, depending on the precision needed.

4.2 Package Outline

Figure 18 and Figure 19 shows the package outlines of the XC822 (TSSOP-16) and XC824 (DSO-20) devices respectively.

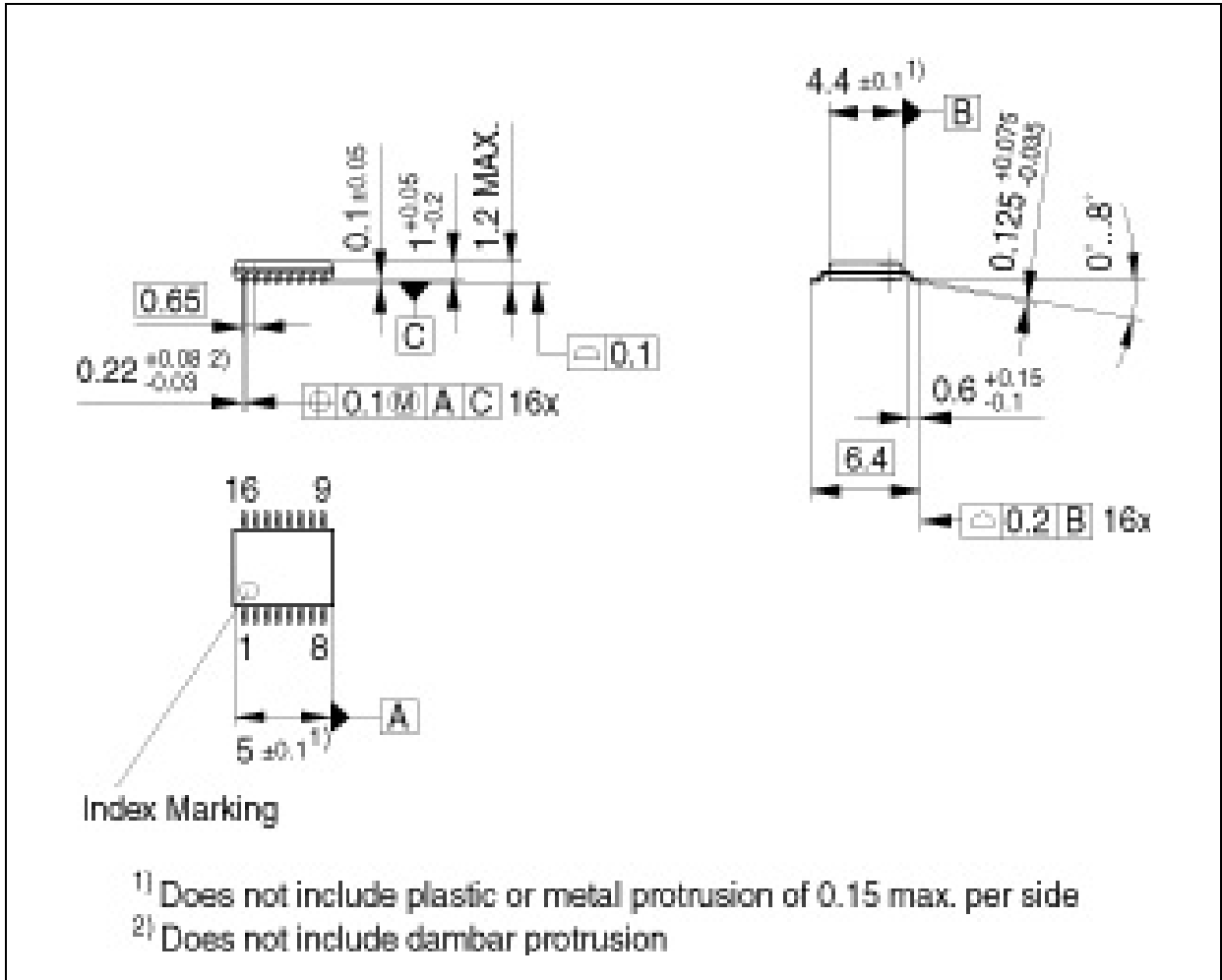


Figure 18 PG-TSSOP-16-1 Package Outline

Package and Quality Declaration

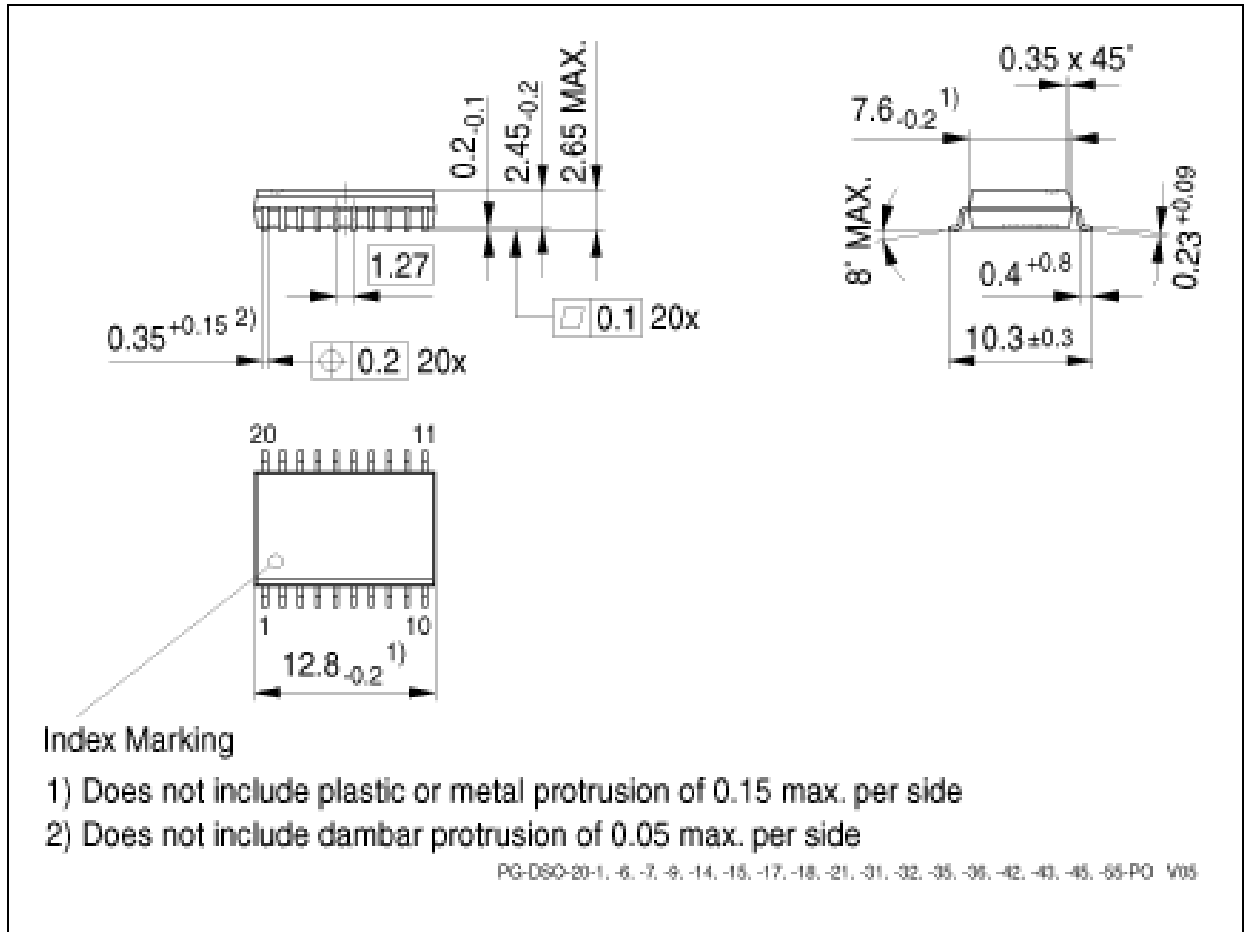


Figure 19 PG-DSO-20-45 Package Outline

4.3 Quality Declaration

Table 25 shows the characteristics of the quality parameters in the XC822/824.

Table 25 Quality Parameters

| Parameter | Symbol | Limit Values | | Unit | Notes |
|--|-----------|--------------|--------|-------|---------------------------------|
| | | Min. | Max. | | |
| Operation Lifetime when the device is used at the three stated T_J ¹⁾ | t_{OP1} | - | 1500 | hours | $T_J = 150^\circ\text{C}$ |
| | | - | 15000 | hours | $T_J = 110^\circ\text{C}$ |
| | | - | 1500 | hours | $T_J = -40^\circ\text{C}$ |
| Operation Lifetime when the device is used at the stated T_J ¹⁾ | t_{OP2} | - | 131400 | hours | $T_J = 27^\circ\text{C}$ |
| ESD susceptibility according to Human Body Model (HBM) | V_{HBM} | - | 2000 | V | Conforming to EIA/JESD22-A114-B |
| ESD susceptibility according to Charged Device Model (CDM) pins | V_{CDM} | - | 500 | V | Conforming to JESD22-C101-C |

1) This lifetime refers only to the time when device is powered-on.

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